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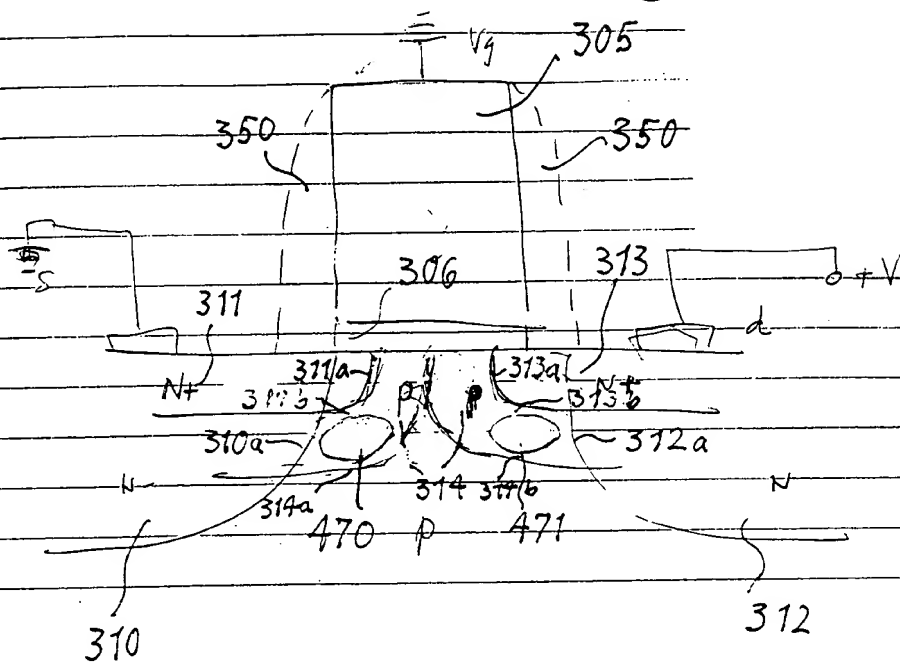


FIG. 4

Isolation

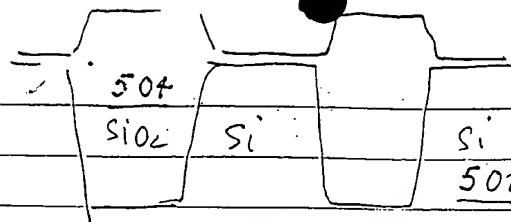


FIG. 5

Vt and well implants

Channel stop

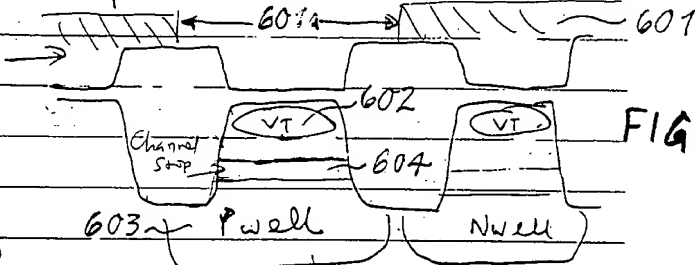


FIG. 6

Gate definition

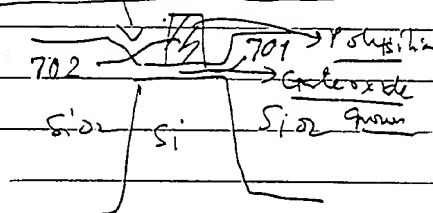


FIG. 7

NMOS & PMOS CDD & Pocket/Heb Implant

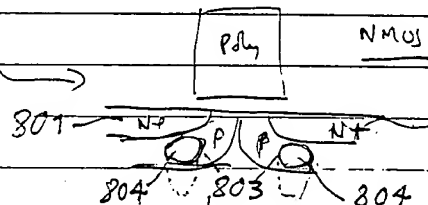


FIG. 8

Spacers & SD Imp

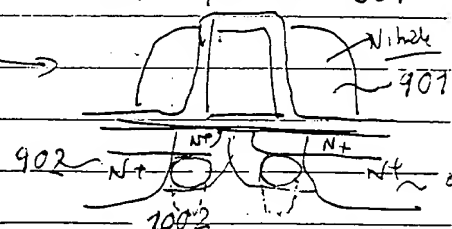


FIG. 9

Silicide formation

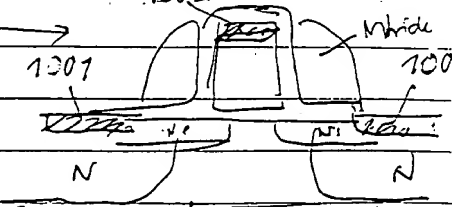


FIG. 10

PMD + Contact formation

Metal deposition pattern